THE REVERSE BIAS REQUIREMENT FOR PIN DIODES IN HIGH POWER SWITCHES AND PHASE SHIFTERS

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ABSTRACT

A key design and cost parameter in a high power PIN diode application is the selection of the applied DC reverse bias voltage. Up to now, this voltage has been chosen either by conservatively using the magnitude of the peak RF voltage or by empirical trials to determine a possible lower value. This paper explores the reverse bias requirement for a PIN diode operating in a high power RF and microwave environment. It demonstrates that the minimum reverse bias voltage is equivalent to the PIN diode's self generated DC voltage under similar RF conditions. An expression for this voltage was developed and experimentally verified that will assist the design engineer in more accurately selecting an appropriate minimum value for the applied reverse bias voltage setting.

INTRODUCTION

A fundamental property of a PIN diode is its ability to control large RF and microwave signals with much lower values of DC current and voltage. While there are design rules for selecting the applied forward current setting based on allowable ohmic loss and distortion requirements [1,2], there are no existing design rules to base the selection of an appropriate applied DC reverse bias voltage setting.

As shown in Figure 1, the instantaneous voltage across the PIN diode (RF and DC) must never exceed its avalanche breakdown voltage or PIN diode failure is likely. Safe operation will result if the instantaneous voltage never forces the PIN diode into forward conduction or into avalanche breakdown. However, this requires that the applied DC voltage to be at least equal to the peak RF voltage. These higher voltages are often not available or too expensive to employ in many applications. In the conditionally safe region there is an instantaneous excursion of voltage into forward conduction. If a reverse voltage in this region is selected, circuit performance factors such as loss, distortion and reliability must not be compromised. It is in this region where most high power (greater than 1 KW) PIN diode switches and phase shifters are designed to operate. The applied DC reverse bias voltage must be large enough to prevent excessive conduction during the positive portion of the RF signal. If excessive conduction does occur, the PIN diode loss will increase and the diode is subject to failure.

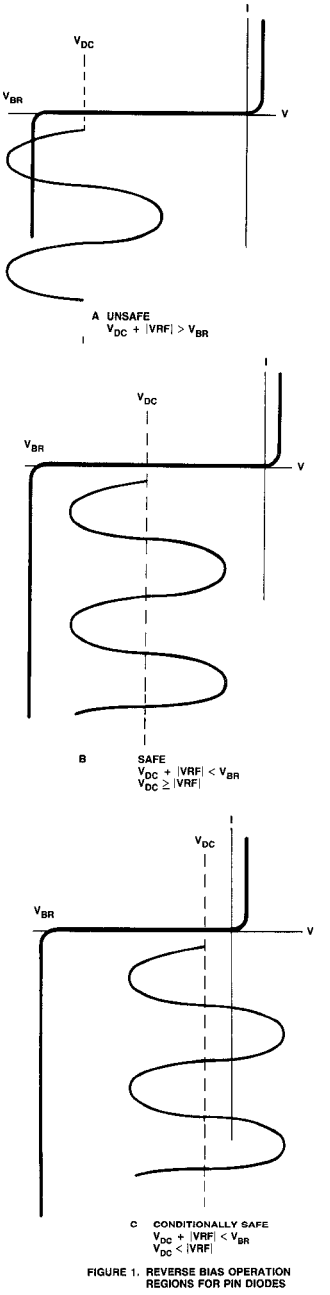

FIGURE 1. REVERSE BIAS OPERATION REGIONS FOR PIN DIODES

In the absence of any theory or analytic design guideline, the designer may choose a DC bias voltage equal to the peak RF voltage resulting in extremely conservative and costly design; alternatively, however, the choice is more frequently based on empirically matching a PIN diode to an available voltage. Published experimental results [3] indicate that the minimum "safe" DC reverse bias needed may be related to frequency and peak RF voltage. This paper presents a concise expression for the safe minimum operating DC reverse bias voltage. It indicates how PIN diode I-region width and circuit parameters such as frequency, duty factor and peak RF voltage affect the selected value of reverse bias voltage.

The investigation of the relationship of the reverse bias requirement and self generated DC voltage was prompted by experimental observations of PIN diode distortion under zero applied bias open circuit conditions, as shown in Figure 2. A self generated reverse bias DC voltage developed across the diode that allowed the device to operate in its high impedance state with good stability. The magnitude of the self generated DC voltage was influenced primarily by the peak RF voltage level, the frequency and the I-region thickness.

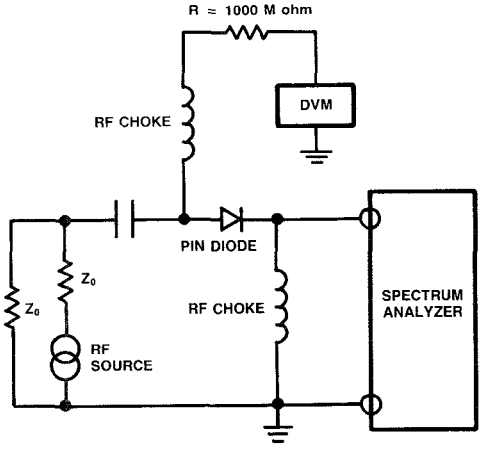

FIGURE 2. MEASUREMENT OF SELF GENERATED DC VOLTAGE

Upon application of an equivalent externally applied DC bias, the distortion generated was identical to self generated voltage. However, when the applied DC voltage was lower than the self generated voltage, unstable performance would occur manifested by large increases in distortion signals and by heating of the PIN diode often leading to device failure.

ANALYSIS

If the PIN diode was an ideal rectifier at RF and microwave frequencies then the DC voltage generated during the negative half-cycle would equal that of the peak applied voltage. The voltage generated by the PIN diode is lower than the applied peak voltage because of its intrinsic region which requires that the RF signal be positive for a finite amount of time before the device starts conducting in the forward direction.

An analysis of the rectification voltage generated by the PIN diode was performed. The analysis was based on the existence of both conduction and displacement currents flowing through the PIN diode [4]:

$$J(t) = 2\,nqv + \epsilon\, dE/dt \qquad (1)$$

where J(t) is the total current density, n is the carrier density , q is the electronic charge, v is the carrier velocity ϵ is the dielectric permitivity and E is the electric field. During each positive portion of the RF voltage, charge is injected into the I-region of the diode by the applied RF signal. Under typical operating conditions, an applied DC reverse bias voltage prevents the movement of this charge across the I-region. If this charge can travel across the I-region during the positive portion of the RF signal (diode transit time less than half the period of the RF signal), then the diode can go into forward conduction. This transit time is a function of the applied RF voltage and I-region thickness; hence thicker PIN diodes will be slower to turn on than thinner diodes in the presence of identical RF voltages.

During the negative portion of the RF cycle, almost all of the charge that was injected during the positive portion of the RF cycle will be extracted. There will, however, be a residual charge left behind that, after several RF cycles, will stabilize and create a high impedance conducting path through the diode. This conduction path is in addition to a displacement current path due to the diode capacitance. It is this high impedance path due to the residual I-region charge that governs the DC characteristics of the PIN diode. It is the corresponding self-rectified DC voltage developed across the PIN diode that must be overcome by the applied DC reverse voltage in order to prevent forward conduction of the PIN diode.

An analysis to predict the value of the self generated voltage was performed. The resulting relationship is based on the rectified voltage that a semiconductor generates as a result of an applied RF signal that is either CW or pulsed. For a pulsed signal, it is assumed that the pulse width is much longer than the period of the RF signal. The expression is as follows:

$$|V_{DC}| = \frac{|V_{AC}|}{\left\{1+\left[\frac{\pi F W^2}{0.95\mu V_{AC}\sqrt{D}}\left(1+\sqrt{1+\left(\frac{0.95\mu V_{AC}\sqrt{D}}{W V_{SAT}}\right)^2}\right)\right]^2\right\}^{1/2}} \quad (2)$$

where V_{AC} is the peak RF voltage, f is the frequency, D is the RF duty cycle, μ is the carrier mobility, W is the I-region thickness and V_{SAT} is the carrier's saturation velocity.

Note that at low frequencies or for thin I-regions or for large AC signals, the DC voltage approaches the amplitude of the AC signal. As frequency increases, the DC voltage decrease as approximately 1/F for a given voltage. The DC voltage is further reduced at lower duty factors. The only parameter directly related to the PIN diode is I-region width.

Equation 3 restates this expression in terms of PIN diode parameters more available to the circuit designer. It is plotted as Figure 3. It assumes a mobility value (μ) of 0.15 m^2/V-sec and a value for saturation velocity (V_{SAT}) of 10^7 cm/sec:

$$|V_{DC}| = \frac{|V_{AC}|}{\left\{1+\left[\frac{.0142 F_{MHz} W^2_{mils}}{V_{AC}\sqrt{D}}\left(1+\sqrt{1+\left(\frac{.056 V_{AC}\sqrt{D}}{W_{mils}}\right)^2}\right)\right]^2\right\}^{1/2}} \quad (3)$$

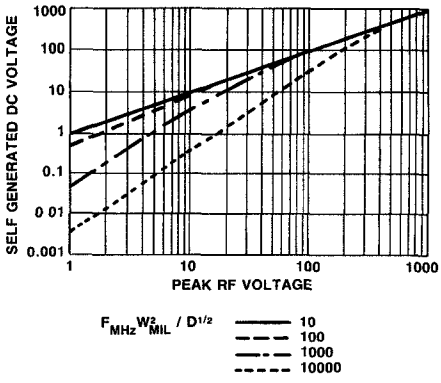

FIGURE 3. SELF GENERATED DC VOLTAGE VS. PEAK RF VOLTAGE

EXPERIMENTAL RESULTS

Experimental measurements of self generated voltage were performed using a test set similar to Figure 2. This test set simulates observing the isolating arm (reverse bias PIN diode) of a SP2T PIN diode in each arm. Measurements were made at power levels up to 100 watts at frequencies from 1 to 60 MHz and duty factors from 0.07 to 1.0. The PIN diode specimens selected had I-region widths from 2mils to 8mils and encompassed various cross section areas and carrier lifetime values. Figure 4 shows good correlation between measured data and analytical expectations from Equation 2 for the ratio of V_{AC} to V_{DC} under the varied conditions.

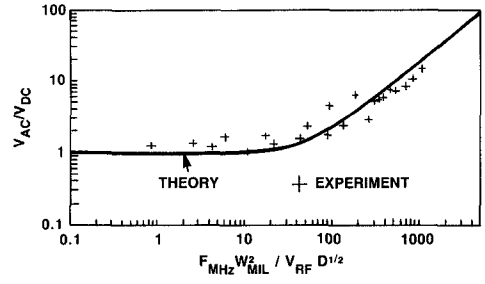

FIGURE 4. COMPARISON OF MEASURED AND THEORETICAL VALUES OF V_{AC}/V_{DC}

A significant experimental observation indicates that the PIN diode may be operated at high RF power without applying any external DC bias. The PIN diode here is operating in a zero bias open circuit mode where the self generated voltage becomes the reverse bias. To operate in this open circuit mode any external resistance across the PIN diode terminals must be very high, generally higher than 100 meg-ohms. Typical levels of harmonic distortion in this mode were approximately 20dB below the carrier.

Upon application of an external DC reverse bias at identical values of the self generated DC voltage the distortion measured was identical. If the applied DC reverse bias were increased slightly, often as little as 10 volts higher than the self generated voltage the distortion would improve significantly as much as 60dB below carrier. If the applied reverse voltage was lower than the self generated voltage, the distortion would degrade often leading to PIN diode failure. The dependence of reverse bias distortion with increasing reverse bias is consistent with observations and experiments done by Caverly and Hiller [5].

It was also observed that the time it took for the self generated voltage to reach its final value was virtually instantaneous upon initial application of RF power. However, when the RF power was changed there appeared to time lag of a few seconds until the DC voltage stabilized and reached its new final value.

APPLICATIONS AND CONCLUSIONS

As a result of this study, the designer may now analytically determine the minimum DC reverse bias requirement for a PIN diode in a high power RF environment. It also affirms that the value of the DC voltage may be significantly lower than the peak RF voltage. The following table indicates the calculated generated DC reverse bias voltage for a PIN diode used as a switch element at 1GHz for a 1KW signal (Vpeak = 316.2 volts across 50 ohms) at different duty factors using PIN diodes of different I-region widths:

Calculated Generated Reverse Bias Voltage

W (mils)	DF=0.01	DF=0.10	DF=1.0
2	73.3 volts	128 volts	155 volts
4	21.0 volts	50.5 volts	77.1 volts
7	7.07 volts	19.9 volts	38.3 volts

The chart indicates that thicker I-region PIN diodes require lower DC reverse voltages and would appear preferably to thinner diodes. It should be noted, however, that thicker PIN diodes may also have higher forward resistance and will switch at a slower speed.

In many situations, the designer is unsure of the exact RF voltage stress on the PIN diodes or its I-region width. The experimental method described in this paper may also be used to measure the self generated DC voltage. This value may then be considered as the minimum applied reverse bias voltage. In many situations the DC voltage established must be able to support RF signals where the SWR of the load termination may increase to infinite SWR. Under this situation, the RF voltage will be double that of a perfectly matched circuit. In applying Equation 2 or 3 the inserted value of RF voltage must reflect the peak value at maximum stress.

It would be a valuable contribution if a circuit technique could be devised that would allow only the application of a small incremental DC reverse voltage to the self generated voltage to obtain distortion performance similar to that of applying the full DC reverse voltage. This would significantly lower the cost of the higher voltage PIN diode drivers presently being designed in higher power switches and phase shifters.

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